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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,515	08/27/2003	Masataka Kusumi	60188-631	3985
20277	7590	12/09/2004	EXAMINER	
MCDERMOTT WILL & EMERY LLP			ORTIZ, EDGARDO	
600 13TH STREET, N.W.			ART UNIT	
WASHINGTON, DC 20005-3096			PAPER NUMBER	
			2815	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/648,515

Applicant(s)

KUSUMI ET AL.

Examiner

Edgardo Ortiz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (Claims 1-3) in the reply filed on October 5, 2004 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as disclosed in figures 10A-19, and their description on pages 2-8 of the instant application, in view of Yuan et al. (U.S. Patent No. 6,512,263). With regard to Claim 1, Applicant's admitted prior art discloses a semiconductor memory device (page 2, lines 4-5) comprising:

a plurality of isolations (202) formed on a semiconductor substrate (201);

a plurality of active regions defined on the semiconductor substrate and isolated from each other by the isolations (figure 15C);

a plurality of control gates electrodes (204) formed over the semiconductor substrate, each said control gate electrode crossing all of the isolations and all of the active regions (figure 15A) with a first insulating film (203) interposed between the control gate electrode and the semiconductor substrate (figure 15B); and

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a plurality of floating gate electrodes (210C), each of which is formed for associated one of the active regions so as to cover a side-face of associated one of the control gate electrodes with a second insulating film (209) interposed between the floating gate electrode and the control gate electrode (figures 15B and 16B),

wherein the isolations are spaced apart from each other along the width of the control gate electrodes (figure 15A) and

wherein each of said isolation crosses all of the control gate electrodes (figure 15A).

Applicant's admitted prior art fails to disclose that the isolations extend continuously along the length of the control gate electrodes. However, Yuan discloses a non-volatile memory cell array, which includes conductive lines (49, 51, 53) that are crossed by isolation trenches (72, 73, 74) that extend continuously along their length (figures 2 and 3).

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include isolations that extend continuously along the length of control gate electrodes, as suggested by Yuan, in order to provide a high-degree of electrical isolation between rows and cells (column 6, lines 14-16), as well as increase the data density of the memory device (column 6, lines 16- 28).

With regard to Claim 2, Applicant's admitted prior art discloses a third insulating film (205) formed on each of the control gate electrodes (204), (figure 15B).

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With regard to Claim 3, Applicant's admitted prior art discloses (figures 15B and 16B) active regions each having a plurality of step-regions (201a), each of which is overlapped by associated one of the floating gate electrodes (210C) and,

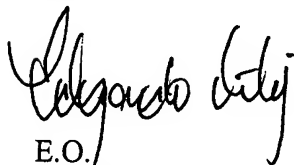
wherein in each of said active regions, source regions (215) are defined in respective upper parts of the step regions and a drain region (214) is defined below the step region (figure 17B).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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